FPGA-Based Simultaneous Multichannel FM Broadcast Receiver for Audio Indexing Applications in Consumer Electronics Scenarios

Brunel Happi Tietche, Olivier Romain, Bruce Denby, *Senior Member*, IEEE, and François de Dieuleveult

Abstract — *The paper describes a Software Defined Radio architecture that simultaneously demodulates all radio stations in the Frequency Modulated (FM) band, and is intended as a preprocessor for content and metadata indexing applications. The system, which contains an overlap-add type channelizing filterbank and a massively parallel frequency demodulation block, is implemented in a single Field-Programmable Gate Array, thus offering the possibility of replacing more traditional media indexing installations containing tens of individual receivers. It is believed to be the first single chip full-band channelization system intended for consumer broadcast media indexing applications. Chip resource utilization details and experimental results from the developed system are also presented*[1].

Index Terms — Software Defined Radio, FPGA, FM, Indexing applications.

I. Introduction

Broadcast radio in the Amplitude Modulation (AM), Frequency Modulation (FM), Digital Audio Broadcasting (DAB), and Digital Radio Mondiale (DRM) bands today contains an enormous amount of information: music; news, sports, and weather services; traffic information; commentary; drama; advertising, of course; and an increasing amount of meta-data (the Radio Data System, RDS, of the FM band, for example) to help identify and organize this content. In most consumer applications, however, the content of radio transmissions remains volatile; that is, once a musical number or a news report has terminated, no tangible trace of the associated content remains.

Media monitoring, in contrast, is the process of capturing, recording, labeling, and analyzing broadcast media content. Companies specializing in this field generally make use of massive installations containing multiple receivers, situated at sites throughout the broadcast area, to keep track of industrial property concerns for their clients, such as statistics on commercial announcements; copyright issues; airplay statistics for musical content; mention and use statistics for company or product names; etc.

Today, Software Define Radio techniques, SDR, and increased logical element counts on Field Programmable Gate Array devices, FPGA, have led to a situation in which one may imagine the power of such a media monitoring installation on a single chip. This advance, in addition to providing media monitoring concerns with more manageable and less expensive solution, also opens to the door to a wealth of exciting new consumer electronics applications.

The ability to capture and demodulate all radio stations in real time in a single, portable device can enable such applications as: interactive, content-aware man-machine interfaces; intelligent navigation of radio content; playlists prioritized according to user tastes; musical genre identification; airtime keyword searches; and a wealth of other possibilities. The design and FPGA implementation of such a system is the main focus of the present article. It focuses on the front end of the system, responsible for capturing and demodulating the radio signals and preparing them for indexation; the audio indexing engine itself will be described in a future article. As FM radio is still a major force in broadcast radio worldwide, the receiver proposed here specifically targets the (European) FM band. The method can of course be used for any similar FM band.

The paper is organized as follows. Section II briefly describes the state of the art concerning the demodulation of multiple channels for broadcast applications. Section III gives a description of the proposed receiver architecture, while the results obtained on the constructed prototype are detailed in section IV. Some discussion and concluding remarks appear in section V.

II. Related Work

The past decade, a number of industrial and academic studies have addressed the problem of the simultaneous demodulation of multiple channels for broadcast applications, based on either an SDR solution or a customized system-on-chip. The two principal design elements of the architecture of the targeted application, an analog front end and a channelizer, are described below.

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Although SDR prescribes sampling as close as possible to the antenna, an analog front end, to filter and amplify the signal, is still typically required. The importance of the front end in SDR-based broadcast applications is shown for example in Kim *et al* [1] and Puvaneswari and Sidek [2], for a DRM+ receiver and a multi-standard receiver, respectively.

Channelizers are systems that can extract multiple narrow-band channels from a wideband digital signal. A variety of techniques have been developed in the past decade, such as the Digital Down Conversion (DDC) approach [3]–[5]; Pipelined FFT (PFFT) [3]; Polyphase FFT filterbanks (PDFT) [3]–[6]; Weighted Overlap and Add filterbanks (WOLA) [3]–[4], [6]; Pipelined Frequency Transform (PFT) [3]; and Tunable PFT (TPFT) [3]. For uniformly spaced channels with identical filtering, the PDFT and WOLA approaches are very efficient in terms of computational complexity when the number of channels is large [3], [6]. DDC allows configuring any center frequency and any filter for the bins, but is suitable predominantly for applications with few channels (typically 4 to 8), beyond which the hardware resource requirements become excessive [3].

A variety of possible architectures for digital multichannel demodulation of broadcast radio signals have been discussed in the literature, however the great majority are not intended for simultaneous demodulation of a large number of stations [7]-[12]. Among those structures designed to handle several FM broadcast channels at the same time, three are of note in the context of possible broadcast monitoring/audio indexing applications. The first is a commercial broadcast recording and logging system [13] based on a 19 inch rack mounted industrial computer that can monitor up to 8 FM radio stations simultaneously and record the audio signal on a hard disk. The second is a commercial device [14] that can extract up to 32 channels from the FM band simultaneously using 32 independent, bandwidth receivers, but which does not demodulate the FM signals, so that an additional device is required for a complete system. The third multi-channel architecture is an FPGA-based FM receiver developed by Romain and Denby [15], which can extract and demodulate up to 32 channels located at a particular fixed set of frequencies. The receiver proposed in the present article builds upon the Romain and Denby's receiver [15] by extending its coverage to the entire FM band.

III. ARCHITECTURE OF THE PROPOSED RECEIVER

The architecture of the proposed receiver is composed of 6 blocks mentioned (see Fig. 1).

A. Analog Front End

The receiver is directly fed by an FM antenna. The analog front end selects the appropriate frequency band by bandpass filtering, and amplifies the received FM signal to make it compatible with the input swing of the ADC that follows. The principal challenge lies in the design of a high gain amplifier with a low noise factor and high third-order intermodulation intercept, IP3. Since the FM band (usually 87.8-108 MHz) can contain some fifty stations spaced on average at 400 kHz, the most important parameters will be gain and linearity, with the main difficulty being the number of simultaneous channels and the required amplitude.

The adopted architecture is shown in Fig. 2. No preliminary frequency transposition is performed. The gain, noise factor and IP3 parameters were optimized without particular attention to power consumption and miniaturization concerns. Simulations carried out with an RF integrated development environment were used to find the optimal configuration of two passive 3rd order Butterworth bandpass filters, two fixed-gain, high linearity amplifiers, and a controlled gain amplifier. The overall gain of the chain is 60 dB, and the dynamic (due to the controlled gain amplifier) is 43 dB. The global 3rd order intercept is 42 dBm, which allows limiting the degradation of the Carrier/Noise ratio to 62 dB at an output level of -10 dBm.

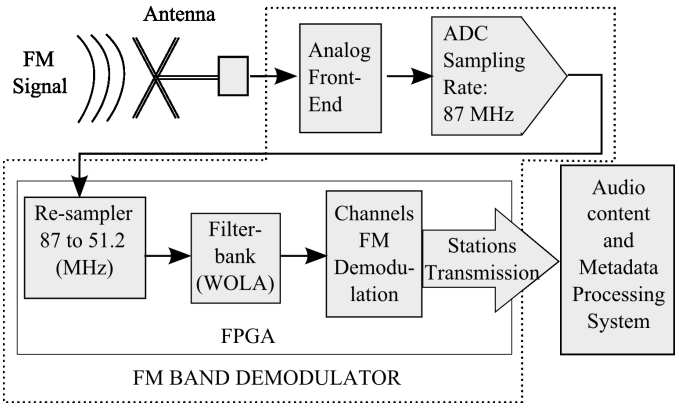

Fig. 1. Synopsis of the architecture of the proposed FM receiver.

B. ADC

As the full FM band must be digitized, the varying signal strengths of the stations must be taken in account. In this article, a maximum difference between strong and weak stations of 55 dB is assumed. To ensure that weaker stations do not disappear beneath the quantization noise floor, and adding another 15 dB noise margin to decode FM satisfactorily, a minimum 12-bit ADC must be chosen. Bandpass sampling at 87 MHz was chosen both to transpose the FM band to baseband, and to limit clock speed demands placed on the subsequent digital processing blocks. The samples obtained are then directly sent to the FPGA for further processing.

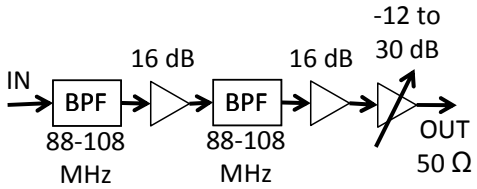

Fig. 2. Overall synopsis of the front end selected.

C. Resampler

Processing architectures with several clock domains generally use a resampling block to change the sampling rate from one domain to one another. Sampled data coming from

the A/D converter are thus immediately dispatched to a resampler block in order to be compatible with the digital processing block of the receiver running at 51.2MHz. A major constraint in the design of the resampling block is the need to keep the level of spurious harmonics generated by the resampling process to a minimum. In particular, these must remain below the 12-bit quantization noise level in order to prevent the masking of weaker stations by spurious harmonics. The problem is illustrated in Fig. 3(a), which gives an example of the very high level of spurious harmonics obtained in a simple resampling process using only a single D flip-flop with no corrections. Fig. 3(b) shows the same signal resampled with the implemented resampler.

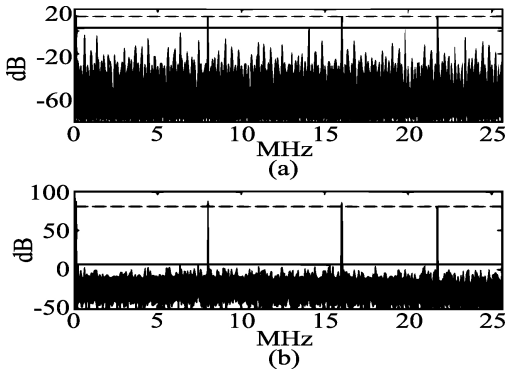

Fig. 3. Spectrum of a 4-carriers sine signal resampled from 87 MHz to 51.2 MHz. The horizontal lines indicate the ratio between the smallest amplitude carrier and the largest harmonics. (a) Resampling using a single 51.2 MHz – clocked DFF (D flip-flop). Spurious harmonics are very prominent. In this example, the ratio is less than 10 dB. (b) Resampling using the proposed resampler block. Spurious harmonics are 73 dB below the signal.

The implemented resampler uses a windowing technique based on a FIR architecture; $2A + 1$ incoming samples are necessary to calculate one output sample. The value chosen for A will determine the signal-to-noise ratio of the output signal. The $2A + 1$ incoming samples consist of $A + 1$ samples preceding the current sample (the sample which is being calculated) plus the A subsequent ones. Coefficients are stored in the $2A + 1$ ROMs, with each ROM corresponding to one incoming sample, as seen in Fig. 4. At each rising edge of the 87 MHz clock, each ROM furnishes the appropriate weighting coefficient for its corresponding incoming sample, and then all weighted incoming samples are summed.

The core of this system is the "Master Control" block (Fig. 4). It precisely controls the incrementation of the ROM indices when a new output sample is to be calculated using the input samples that arrive in the registers. Master Control also avoids FIFO overflow. Indeed, Fig. 4 shows that if a data word is stored in the FIFO on every rising edge of the 87 MHz clock, the FIFO will overflow, since 87 > 51.2. To avoid this, Master Control ensures that only valid output samples enter the FIFO via the "FIFO Write Request" signal.

To make Master Control fulfill these two roles, the "Fractional time interval", μ_k, between an output sample k and the input sample m_k that immediately precedes it is exploited. As k increases from 0 to $+\infty$, μ_k values are repeated with period 256, since the signal resampling is from 87 MHz to 51.2 MHz and 87 / 51.2 = 435 / 256.

Master Control keeps in memory a simplified "resampling map", which is a binary vector of length 256 based on μ_k values. Master Control uses this map to increment the ROM indices at the appropriate time and assign the "FIFO Write Request" signal which allow the summation result to be sent into the dual clock FIFO as needed. A mathematical software package was used to determine the appropriate map values to store.

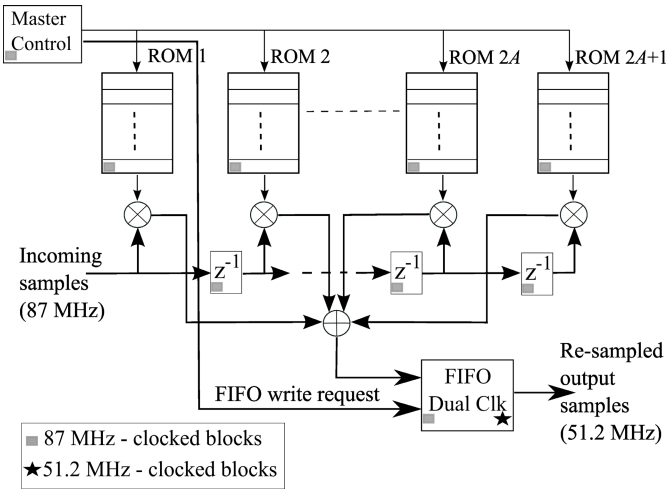

Fig. 4. Resampling system. The ROMs store weighting coefficients used to interpolate incoming samples.

The coefficients stored in the ROMs are obtained via the following two observations:

1) Only one period of μ_k, which corresponds to 256 coefficients per ROM, is stored. The i^{th} coefficient of the j^{th} ROM weights the incoming sample that corresponds to the j^{th} ROM at the i^{th} μ_k instant of one period.
2) In the current application, the spurious harmonics must be under the quantification noise (72 dB).

The coefficients are obtained from a 17 coefficient FIR *sinc* lowpass filter, windowed with a Blackman Harris function, as it fits this latter criterion while having a pass band compatible with the FM input signal. The coefficients of this filter are calculated for each μ_k value, quantized on 12 bits and allocated to the $2A + 1$ ROMs, with $A = 8$.

Several bench tests have been performed to obtain the performance of this IP. The spectrum of a 4-carriers sine signal resampled from 87 MHz to 51.2 MHz is showed in Fig. 3(b). Spurious harmonic are 73 dB below the signal.

D. Filterbank Engine

The simultaneous demodulation of the entire FM band requires that all the possible stations to primarily be separated (i.e. filtered and transposed to baseband). Channelization techniques optimized for uniformly spaced channels with identical filtering are predominantly FFT-based (PFFT, PDFT, WOLA, etc.) as mentioned in section II.

The PFFT technique, which processes the input signal directly with an FFT, requires weighting the input signal with a Finite Impulse Response (FIR) low pass filter to improve filtering performance. The FIR "weighting" must be performed before the FFT processing; otherwise, the filterbank's rejection at the first sidelobe will be less than 20 dB, since the FFT impulse response approximates a rectangular window, whose Fourier transform is a *sinc* function, with a first side lobe at only -13 dB. This window can be excessively large if the required rejection is high, thus necessitating a huge amount of computational resources. As this will be the situation for perfectly isolated FM channels, the use of PDFT [3] or WOLA [3]-[4] is preferable here in order to better manage hardware resources.

Let h(n) be the input filter's impulse response of length L, D the sampling rate decimation factor between the original signal and generated outputs, and K the number of channels to be generated by the filterbank. The basic PDFT [3] structure uses the same number of multipliers as the windowing version of the PFFT discussed above; however, its polyphase implementation allows it to work at much higher frequencies than the PFFT filterbank. The implementation of the PDFT in this basic form requires the creation of as many filters as channels to be processed. This drawback can be circumvented by preferring a more sophisticated PDFT structure, equivalent to implementing a WOLA algorithm when $D = K$ and L is multiple of K.

The implemented channelizer uses this WOLA - or "improved" PDFT – architecture (Fig. 5). The number of multipliers required is far lower than what a basic PDFT would have required. Indeed, excluding the FFT, the basic PDFT [3] requires L multipliers, whereas WOLA needs only L / K. This WOLA implementation is also well adapted to the data acquisition mode of standard FFT IP cores used in FPGA implementations, which usually sends and receives its data in a serial fashion. Thus, the input data samples $x^I_0(m)$, $x^I_1(m)$.. $x^I_{K-1}(m)$ are sent one per clock cycle, the output samples are generated in the same way, that is, consecutively in the order, $X_0(1)$, $X_1(1)$..$X_{K-1}(1)$, $X_0(2)$, $X_1(2)$...$X_{K-1}(2)$, $X_0(3)$, $X_1(3)$... $X_{K-1}(3)$…(Fig. 5).

The filterbank pass band width is set to the FM signal maximal frequency deviation. For that, an L = 4096-sample Kaiser filter with a rejection of 60 dB has been retained.

The WOLA filterbank transposes each extracted channel to baseband. Let F_i be the extracted channel sampling rate. By Shannon's theorem, $F_i / 2 \geq$ must be superior or equal to 100 kHz. Furthermore, in many countries, FM station centres occur at 87.5 + $i \times 0.1$ (MHz), where $i \in \{0, 1, 2 \ldots 205\}$. As the filterbank will create outputs for these stations, it should also, in principle, respect this 0.1 MHz spacing.

In practice, this may not be possible due to material constraints, as expressed by the following set of conditions. According to the Nyquist criterion, $F_{SFM} / 2 \geq B_{FM}$, where F_{SFM} is the sampling rate of the FM signal to channelize and B_{FM} the width of the commercial FM band. B_{FM} is generally equal to 20 MHz. As $F_{SFM} = D \times F_i$ and $F_i / 2 \geq 100$ kHz, F_{SFM} must be superior or equal to $2 \times D \times 100$ kHz. The number of channels output by the FFT IP core is K and $D = K$. Now, the K output channels are not independent. Indeed, the number of independent channels output by the FFT IP core is $K / 2$ because the FFT IP core outputs the negative and the positive frequency component samples of one independent channel per output frame. Let j be a positive integer so that $j \times 0.1$ MHz is the spacing between centers of extracted channels. One may deduce that $(F_{SFM} / 2) / (K / 2) = j \times 0.1$ MHz due to the filterbank, where $F_{SFM} / 2$ refers to the bandwidth that must be processed and $K / 2$ gives the number of useful extracted channels. Furthermore, the FFT IP core forces $K \in \{64, 128, 256 \ldots 16384\}$. The conditions on F_{SFM} mentioned above are listed, after simplification, in (1), where F_{SFM} the unit of is MHz.

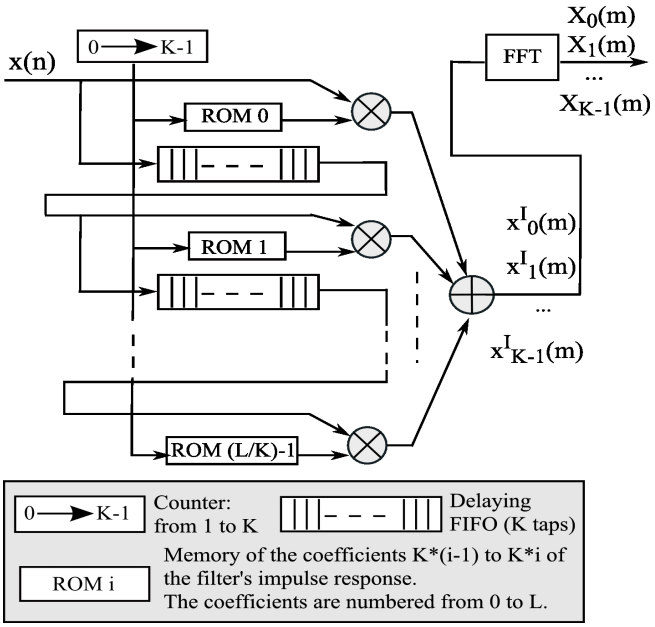

Fig. 5. WOLA implementation when D = K and L is a multiple of K. In this structure, all the blocks are clocked at the same frequency. Each "Delaying FIFO" delays the "x(n)" samples from K clocks instants. The "ROM I" blocks have K memory cells, numbered for 1 to K. The counter block, which index the each "ROM I" block, counts from 1 to K in an infinite loop.

$$F_{SFM} \geq 40; \quad F_{SFM} \geq 0.2 \times D; \quad F_{SFM} / K = j \times 0.1 \qquad (1)$$

Table I shows that there are many possible combinations of j, K and F_{SFM} that could satisfy the conditions listed in (1).

TABLE I
SOME POSSIBLE VALUES OF F_{SFM} IN MHZ

K (or D)	K / 2	j = 1	j = 2	j = 3	j = 4	j = 5	…
64	32	6.4	12.8	19.2	25.6	32	…
128	64	12.8	25.6	38.4	51.2	64	…
256	128	25.6	51.2	76.8	102.4	128	…
512	256	51.2	102.4	153.6	204.8	256	…
…	…	…	…	…	…	…	…

Note that grey background cells denote unauthorized possibilities since F_{SFM} must be greater than 40 and j > 1.

Now, a filterbank that satisfies the following additional conditions has been implemented:

1) The lowest permissible clock frequency. Indeed, FPGA designs often have a maximal clock frequency above which the good functioning of the design is not guaranteed.
2) Most efficient use of hardware resources. It was discovered in the early prototyping phase that filterbank engines with lower K lead in general to increased hardware resource utilization.
3) Good audio quality. It was also determined empirically that lower K values lead to better audio quality of the demodulated FM stations, presumably because more samples per hertz of output audio waveform are retained.

The parameter set, $K = D = 128$, $j = 4$ and $F_{SFM} = 51.2$ MHz, is a good compromise given the conditions mentioned above. The set $j = 4$ leads the implemented filterbank to be 400 kHz-equispaced, as $j \times 4 = 0.4$ MHz.

In order to implement this solution using the chosen parameter set, the proposed architecture thus incorporates a resampling block (described in section III-C) that changes the sampling rate of the signal from 87 MHz to 51.2 MHz so that $F_i = F_{SFM} / D = 400$ kHz.

The outlined 400 kHz-spaced filterbank cannot extract any set of stations in the FM band, indeed neither can any WOLA implementation having $j > 1$, as some stations may be centered at frequencies where there is no filterbank bin. The solution adopted to address this issue is to simply add additional interleaved WOLA filterbanks in parallel as shown in Fig. 6.

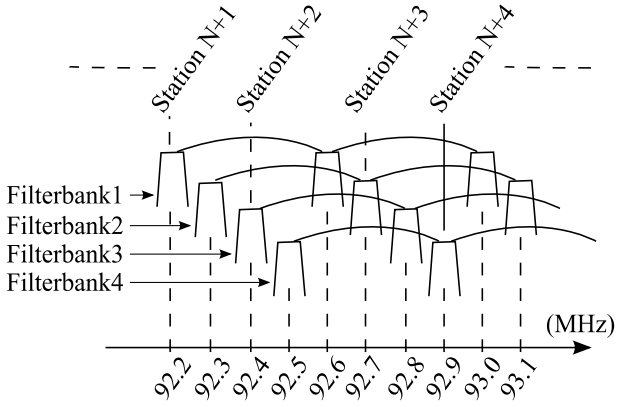

Fig. 6. Example of distribution of stations in the FM band and filterbank system for interleaved channel extraction.

A straightforward way to create the interleaved filterbanks is to create copies of the input signal shifted by 0, 100, 200 and 300 kHz, and send the resulting signals to separate copies of the WOLA filterbank. The final filterbank engine is then composed of 4 branches (indicated by branches 1, 2 3 and 4 in Fig. 7) where branches 2, 3 and 4 integrate a numerically controlled oscillator (NCO) that produces a sine signal used to frequency – shift the input signal. The standard NCO and FFT IP cores provided in the FPGA design development software package were used for the receiver.

E. Massively Parallel Frequency Demodulators

Once all the modulated channels are extracted, the next step is to demodulate them. Since the filterbank system is made of 4 interleaved branches, with each branch extracting 128 channels spaced at a 400 kHz interval (of which, again, only half are unique), the number of distinct channels that the filterbank system outputs will be $4 \times 128 / 2 = 256$. Two possible implementations of the demodulation system become possible:

1) Generate 256 instances of the demodulation system working in parallel.
2) Pipeline the demodulation system so that a single module suffices to demodulate all the channels of a given branch.

The first choice is obviously the simplest for our application, since FPGAs are designed for parallelized structures. Unfortunately, the cost in terms of logic registers or DSP blocks quickly can reach the limits of available FPGA resources. In order to minimize this cost, the second alternative has been chosen.

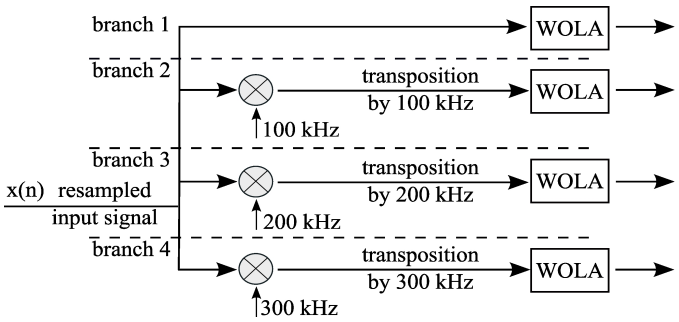

Fig. 7. 4-branch filterbank system. The NCOs are represented by the frequency of the sine signal they produce.

Two popular frequency demodulation techniques are suitable for FPGA-based demodulators and pipelined techniques. These are the differentiate-divide approach and the arctangent-differentiate approach [16]. Equations (2) and (3) respectively characterize them.

$$Y = \left(I.dQ / dt - Q.dI / dt\right) / \left(I^2 + Q^2\right) \tag{2}$$

$$Y = d\left(Arc\tan\left(-Q / I\right)\right) / dt \tag{3}$$

where the calculation of arctangent in (3) can be done with the CORDIC algorithm [17]-[18].

When the sample rate is close to the maximal frequency deviation, as in the current application, the arctangent-differentiate method gives better results than the differentiate-divide demodulation unless this latter integrates a sophisticated filter, which renders pipelining difficult. Thus the demodulator set for the proposed receiver is the arctangent-differentiate.

The arctangent function in (3) is intended as a four-quadrant operation. In practice, however, a CORDIC calculation block evaluates the value of a one-quadrant angle,

i.e., an angle in the range [0, π/2], by calculating the function arctan(-Q / I). In the proposed implementation, the CORDIC block is preceded by a block that first transposes any angle to the interval [0, π/2]. This block (called "four-quadrant to one-quadrant") assigns a signal (denoted "control signal") which retains the index of the original quadrant of the angle being treated.

Once the angle becomes a one-quadrant angle, the CORDIC block performs the calculation of arctan(-Q / I), outputting the value of the angle in [0, π/2]. The angle calculated is then sent to subsequent block, "one-quadrant to four-quadrant" (Fig. 8), which brings the angle calculated back to its original quadrant.

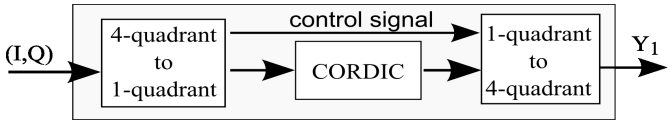

Fig. 8. CORDIC-based Arctan calculation system. "Control signal" tells to "1-quadrant to 4-quadrant" block which quadrant the angle generated by the "CORDIC" block belongs to.

The derivative function in (3) must employ an "unwrap" operation in order to assure phase continuity. Indeed, the arctangent block produces angles between 0 and 2π, and thus discontinuities between two consecutives angles are possible. For example, the derivative of the two consecutive angles 5π/2, 3π/4, which should give 5π/2 - 3π/4 = 7π/4, will rather give π/2 - 3π/4 = -π/4 because the arctangent calculation maps 5π/2 to π/2. Although these represent the same angle on the unit circle, their overall phase values are different. Correct angle values are very important here because they contain the FM radio output data of the entire system. The "unwrap" block offers a solution to this problem. Let $Y_{1,N}$ and $Y_{1,N-1}$ denote consecutive angles produced by the arctangent block. The "unwrap"-based differentiation function makes use of the fact that the difference between $Y_{1,N}$ and $Y_{1,N-1}$ will always be less than π, since the signal is sampled at 400 kHz and the FM radio maximal frequency deviation only 100 kHz.

The CORDIC algorithm is iterative. In a system with no timing constraints, such as a calculator, one may perform as many iterations as needed until the desired precision is reached. In a real-time system such as an FPGA-based design, however, a maximum number of iterations must be imposed, depending on available hardware resources. The pipelined demodulator structure takes advantage of this fact. Indeed, using the fact that there are a fixed number of iterations, the CORDIC algorithm is decomposed so that each iteration becomes a single block, as shown in Fig. 9. In this way, all I-Q pair samples arriving at the CORDIC block are processed independently, thus avoiding any delay, regardless what channel they belong to. Consequently, the corresponding angle is calculated from each pair-sample, without any delay being incurred in the process.

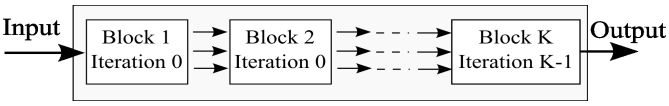

Fig. 9. Decomposition of CORDIC algorithm in blocks.

Once the angle calculated, the last step is to differentiate the obtained angles. As a simple differentiator is chosen, a buffer has been added to the system in order to delay samples so that the differentiator block receives 2 consecutives samples from a given channel simultaneously (Fig. 10).

F. Demodulated Stations

The demodulated channels are transferred via a serial connection to the audio content and metadata processing system. Such a system can of course be implemented on an FPGA, Graphics Processing Unit (GPU), Central Processing Unit (CPU), Multi-Processor System-on-Chip, or any hardware system able to process the signals in an appropriate way. In order to keep clock speed as low as possible, only those channels that actually contain a radio station are transmitted. For example, in the Paris metropolitan area, 51 FM radio stations have been catalogued. Rather than transferring all 206 demodulated channels, in this case, only these 51 are transmitted. This approach reduces constraints on clock rate and allows using an USB2 connection.

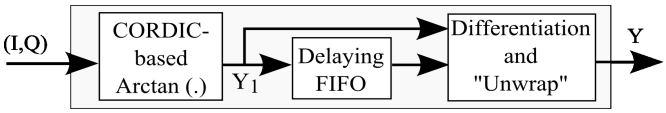

Fig. 10. Pipelined arctangent-differentiate demodulator structure.

IV. PROTOTYPE AND RESULTS

A. Prototype

The complete receiver is obtained by assembling the described blocks. A photo of the system is given in Fig. 11.

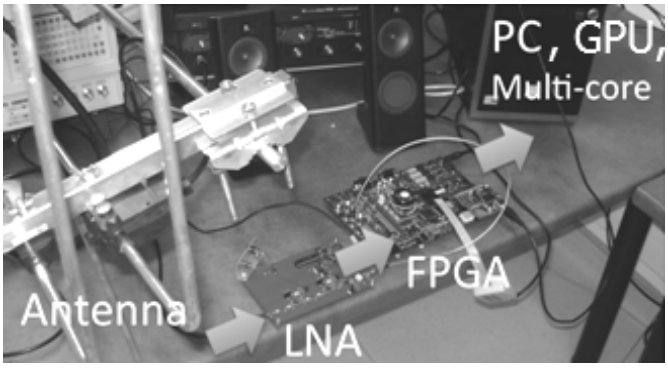

Fig. 11. Overall view of the prototype including antenna, analogue front end (LNA), FM band demodulator (FPGA), and audio content and metadata processing system (GPU).

The FPGA resource utilization [19] of the prototype is summarized in Table II. The contribution of each block of the system is individually given by Table III.

B. Experimental Results from the Prototype

The output audio spectrum of a typical French FM station, after the full chain of processing by the prototype, is presented in Fig. 12(a). Fig. 12(b) gives an example of FM spectrum use for France, to aid in the interpretation of the experimentally obtained spectrum above it. The monaural and stereo bands, as well as the standard 19 kHz synchronization pilot and RDS band, are very clearly distinguished in the experimental spectrum from the prototype. The device simultaneously provides such an output for all FM radio stations present in the local reception area.

A SNR measurement gives a further handle on the quality of the audio produced by the prototype. The experimental process to obtain its value is as follows. An arbitrary demodulated channel was chosen, and the FPGA programmed to output this channel on a stereo jack connector driven by an Audio coder/decoder (CODEC) available on the FPGA board. The output demodulated signal level at the jack connector when no FM signal is input is then measured. This becomes the measured system noise level. Subsequently, for different gains of the front-end and different levels of a 1 kHz-carrier, frequency modulated with a deviation of ± 75 kHz (as for a standard FM radio station), the level of the demodulated output signal is measured. The SNR is then calculated from these measures.

TABLE II
RESOURCE UTILIZATION OF THE PROTOTYPE

ALUTs	67,999 / 143,520 (47 %)
Dedicated logic Registers	64,950 / 143,520 (45 %)
Total Registers	64950
Memory bits	2,275,985 / 9,383,040 (24 %)
9-bit DSP blocks	454 / 768 (59 %)
Max 87	163.72
Max 51.2	116.93

The percentages of available chip resources used. Max 87 and Max 51.2 are respectively the maximal 87 MHz-clock authorized and the maximal 51.2 MHz-clock authorized.

TABLE III
CONTRIBUTION OF EACH BLOCK

	Contribution of each block described above according to the resources used by the entire prototype, apart from "dynamic adapter"				Contribution of the remaining parts (%)
	Re-sampler (%)	Filter-bank (%)	Frequency demodulator (%)	stations transmission system (%)	
ALUTs	0.52	77.22	6.68	14.17	1.41
DLRs	0.9	79.14	6.5	11.81	1.65
Total Registers	0.9	79.14	6.5	11.81	1.65
Memory bits	2.97	38.21	0.33	49.68	8.81
DSP block 9 bit	7.49	92.51	0	0	0
Max 87	163.91				
Max 51.2	296.47	108.64	193.05	149.54	

Percentages of total resources for each block; and logic and memory used to connect the blocks. DLRs are the dedicated logic registers. Max 87 and Max 51.2 are respectively the maximum 87 MHz- and 51.2 MHz-clocks.

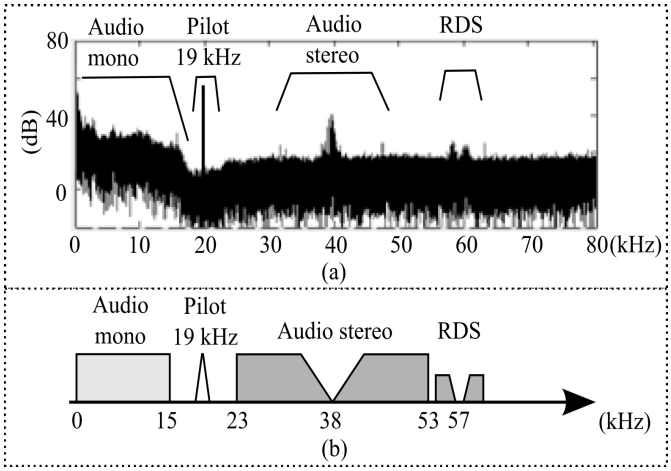

Fig. 12. (a) Spectrum of a French radio station demodulated by our prototype. (b) Information allocation in a French standard FM spectrum of a radio.

Results appear in Fig. 13, which shows the SNR for audio noise as a function of the FM modulated RF signal input level. The curves indicate that the proposed receiver prototype is capable of achieving an SNR of 50 dB, which is comparable to that obtained in traditional analog receivers.

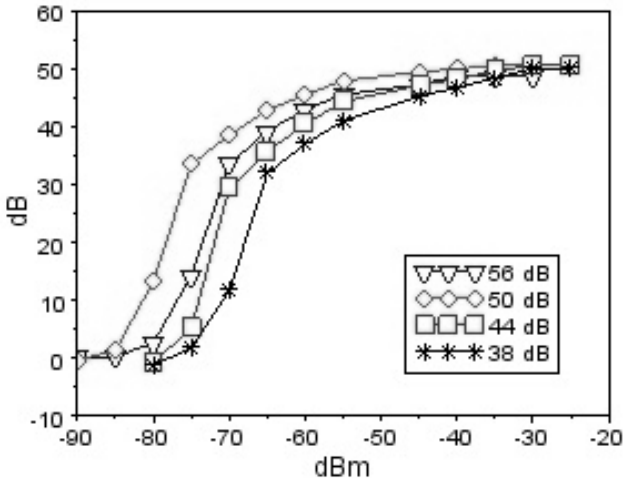

Fig. 13. SNR given by the prototype versus input signal level. The values in the rectangle are the different pre-amplifier gains of the front-end.

Where the proposed receiver comes up somewhat lacking, however, as compared to an analog receiver, is in regard to its overall RF sensitivity. Indeed, traditional receivers can maintain sensitivity down to -90 dBm [20], whereas the prototype cuts off around -80 dBm, depending on the pre-amplifier gain. This deficiency however is to a certain extent determined by the least count (12 bits), and could in principle be improved by: using two ADCs, one for high power stations and another, accompanied by a dedicated analog circuit, for lower power ones, as proposed by Ihmig, and A. Herkersdorf [7]; or by simply using an ADC of more than 12-bit precision.

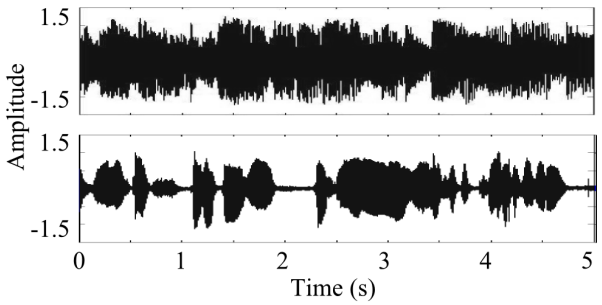

Fig. 14. Waveforms of two radio stations logged at 200 kHz over a period of five seconds. The top recording was made while jazz music was being broadcast, while the lower one shows a waveform for a speech broadcast.

The stations output by are intended for subsequent use in audio indexing applications in consumer electronics scenarios, for example, speech/music detection, music genre identification, speech processing, and the like. To get an intuitive idea of the viability of such applications, Fig. 14 provides the waveforms of the mono component of two radio stations, logged at 200 kilosamples per second, whose programs are quite different for the period examined (five seconds; the stereo, RDS, and 19 kHz pilot components of the FM signal have been removed by filtering for clarity). It is clear from the figure that speech and music waveforms are quite different. The music waveform maintains higher envelope values for longer periods of time, for example, as compared to the speech waveform. This and other differences can be successfully exploited in online audio indexing applications using standard spectral features, such as Mel-Frequency Cepstral Coefficients, MFCC, along with classifier systems [21]. Some preliminary indexing results on data from the prototype have already been published [22]. A more complete treatment of audio-indexing in the context of the prototype is the subject of an upcoming companion article.

V. CONCLUSION AND PERSPECTIVES

An FPGA-based Software Defined Radio architecture that simultaneously demodulates all stations in the FM radio band was presented, with each station demodulated above Nyquist rate, so that all content and meta-data present in the FM radio signal before acquisition is preserved and can be fully exploited in a subsequent audio indexing stage. The originality of the approach arises from:

1) The novel combination of a multi-branch approach to the WOLA filterbank and a pipelined version of the CORDIC algorithm on a single chip.
2) A practical, arbitrary-ratio *sinc*-based sample rate conversion module (a more detailed description of the sample rate conversion module appears in another publication in preparation).

The architecture developed is operational on an FPGA [19], and is currently being tested on a set of benchmark audio indexing applications, the results of which will be the subject of an upcoming article. As our prototype uses only 24% of memory resources (Table II), it should be possible to include additional functionality on the same chip, for example, the implementation of the entire multichannel receiver and audio indexing engine on a single FPGA, for a mobile application. A future work will be about other radio standards beyond FM, including the digital broadcasting standards which have begun to replace the AM and FM bands in many parts of the world, and particularly to Digital Radio Mondiale, DRM (and DRM+).

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BIOGRAPHIES

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